In the Claims

Please amend the claims as follows.

Claims 1-26 (canceled).

Claim 27 (new): A system comprising:

a. a multi-PAM output driver having a plurality of current-control ports;

b. a current-calibration circuit coupled to each of the current-control ports, the current-calibration circuit including a first, second, and third reference-voltage nodes; and

c. a multi-level voltage generator including:

i. a voltage divider having first, second, third, and fourth resistors coupled in series to divide a reference voltage into a first multi-PAM reference voltage between the first and second resistors and coupled to the first reference-voltage node, a second multi-PAM reference voltage between the second and third resistors and coupled to the second reference-voltage node, and a third multi-PAM reference voltage between the third and fourth resistors and coupled to the third reference-voltage node; and

ii. an active current source having a current-handling terminal and a current-control terminal, wherein the current-handling terminal is coupled between two of the first, second, third, and fourth resistors.

Claim 28 (new): The system of claim 27, wherein each of the current-control ports receives at least one current-control bit generated by the current-calibration circuit.

Claim 29 (new): The system of claim 27, wherein the first multi-PAM reference voltage between the first and second resistors is coupled to the first reference-voltage node via an amplifier.

Claim 30 (new): The system of claim 27, wherein the active current source conducts an offset

current, responsive to a current-control signal on the current-handling terminal, based on crosstalk settings.

Claim 31 (new): The system of claim 30, wherein the output driver includes an output terminal coupled to a termination resistor of impedance Z_O, and wherein the offset current is proportional to a product of the impedance Z_O and at least one of a crosstalk current, and an equalization current.

Claim 32 (new): The system of claim 27, wherein the output driver is a four-PAM driver.

Claim 33 (new): The system of claim 27, wherein the first reference-voltage node exhibits a high reference voltage V_{REFHI}, the second reference-voltage node exhibits a medium reference voltage V_{REFMI}, and the third reference-voltage node exhibits a low reference voltage V_{REFLO}, and wherein the active current source is coupled to the first reference-voltage node to reduce the high reference voltage V_{REFHI}.

Claim 34 (new): The system of claim 33, wherein the active current source reduces the high reference voltage V_{REFHI} in response to at least one of an equalization current control signal and a crosstalk current control signal.

Claim 35 (new): A current-calibration circuitry for a multi-PAM output driver, the current-calibration circuitry comprising:

a. a current-calibration circuit including a first, second, and third reference-voltage nodes adapted to receive respective relatively high, medium, and low reference voltages; and

b. a multi-level voltage generator adapted to produce the high, medium, and low reference voltages, the voltage generator including:

   i. first and second voltage supply pins providing a reference voltage;

   ii. a voltage divider having first, second, and third multi-PAM reference terminals, the voltage divider dividing the reference voltage into a

plurality of multi-PAM references, including a first multi-PAM reference voltage on the first multi-PAM reference terminal, a second multi-PAM reference voltage on the second multi-PAM reference terminal, and a third multi-PAM reference voltage on the third multi-PAM reference terminal; and

ii. an active current source drawing current from the first multi-PAM reference terminal to reduce the first multi-PAM reference voltage.

Claim 36 (new): The system of claim 35, wherein the active current source reduces the current is an offset current proportional to at least one of an equalization current and a crosstalk current.

Claim 37 (new): The system of claim 35, wherein reducing the first multi-PAM reference voltage reduces at least one of the second and third multi-PAM reference voltages.

Claim 38 (new): The system of claim 35, wherein the first multi-PAM references voltage is higher than the second and third multi-PAM reference voltages.

Claim 39 (new): A method of calibrating a multi-PAM output driver adapted to cause an output signal to transition between a plurality of logic states, the method comprising:

a. dividing a reference voltage into a plurality of multi-PAM reference voltages on respective multi-PAM reference-voltage nodes; and

b. shifting the logic states to allow equalization signals to overdrive transitions between the logic states, wherein shifting the logic states includes shifting the multi-PAM reference voltages by drawing an offset current from one of the multi-PAM reference-voltage nodes.

Claim 40 (new): The method of claim 39, further comprising developing a current-control signal based upon an equalization coefficient for the output driver to define the offset current.

Claim 41 (new): The method of claim 39, further comprising developing a current-control signal based upon a crosstalk coefficient for the output driver to define the offset current.